# SGS-THOMSON MICROELECTRONICS

MC3479C

STEPPER MOTOR DRIVER

- SINGLE SUPPLY OPERATION + 7.2 V TO + 16 V
- 350 mA/ COIL DRIVE CAPABILITY
- BUILT IN FAST PROTECTION DIODES
- SELECTABLE $\overline{CW}$/CCW AND $\overline{FULL}$/HALF STEP OPERATION
- SELECTABLE HIGH/LOW OUTPUT IMPEDANCE (HALF STEP MODE)
- TTL/CMOS COMPATIBLE INPUTS
- INPUT HYSTERESIS : 250 mV TYP.
- PHASE LOGIC CAN BE INITIALIZED TO PHASE A
- PHASE A OUTPUT DRIVE STATE INDICATION
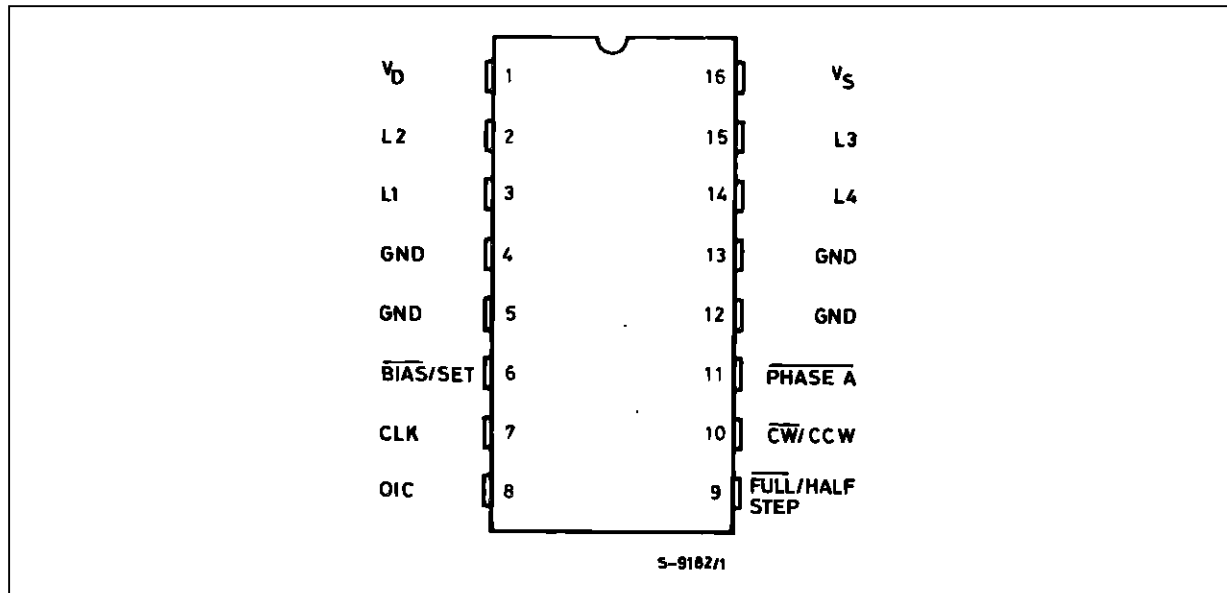
**Powerdip
12 + 2 + 2**

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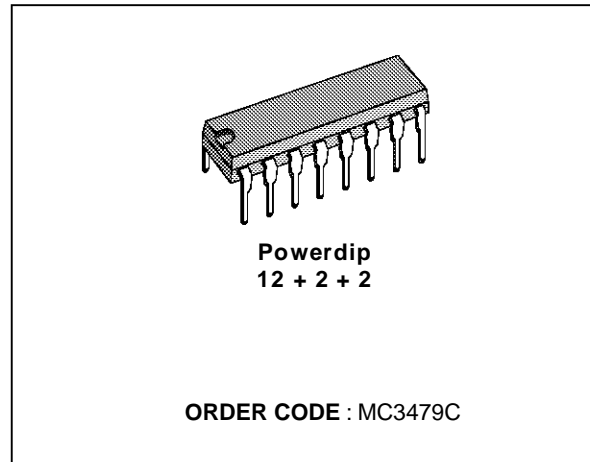
DESCRIPTION

The MC3479C is designed to drive a two-phase stepper motor in the bipolar mode. The circuit consists of four input selections a logic decoding/sequencing section two driver stages for the motor coils and an output to indicate the Phase A drive state.

INPUT TRUTH TABLE

	INPUT LOW	**INPUT HIGH**
$\overline{CW}$/CCW	CW	CCW
$\overline{F}$/HS	Full Step	Half Step
OIC	High Z	Low Z
CLK	Positive Edge Triggered	

PIN CONNECTION

Left	Pin		Pin	Right
V$_D$	1		16	V$_S$
L2	2		15	L3
L1	3		14	L4
GND	4		13	GND
GND	5		12	GND
$\overline{BIAS}$/SET	6		11	PHASE A
CLK	7		10	$\overline{CW}$/CCW
OIC	8		9	$\overline{FULL}$/HALF STEP

S-9182/1

PIN DESCRIPTION

Symbol	Name	Pins	Description
V_S	Power Supply	16	Power Supply pin for both the logic circuit and the motor coil current. Voltage range is 7.2V to 16V.
GND	Ground	4-5-12-13	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins dissipating heat from within the package.
V_D	Clamp Diode	1	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16 (see Figure 5).
L1, L2 L3,L4	Driver Outputs	2-3 14-15	High current outputs FOR the motor coils. L1 and L2 are connected to one coil and L3, L4 to the other coil.
$\overline{B}$/S	$\overline{Bias}$/Set	6	This pins is typicaly 0.7V below VS. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (IBB < 5.0mA) the outputs assume a high impedance condition while the internal logic presets to a Phase A condition.
CK	Clock	7	The positive edge of the clock input swiches the outputs to the next position. This input has no effect if Pin 6 is open.
$\overline{F}$/HS	$\overline{Full}$/Half Step	9	When low (logic 0) each clock pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one-half step (see Figure 4 for sequence).
$\overline{CW/CCW}$	$\overline{Clockwise}$/Counter Clockwise	10	This input allows reversing the rotation of the rotation of the motor (see Figure 4 for sequence).
OIC	Out Impedance Control	8	This input is relevant only in the half step mode (Pin 9 > 2V). When low (logic 0) the two driver out of the non-energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance reference to V_S (see Figure 4).
$\overline{Ph\ A}$	$\overline{Phase\ A}$	11	This outputs indicate (when low) that the driver outputs are in the phase A condition (L1 = L3 = V_{OHD} ; L2 = L4 = V_{OLD}).

BLOCK DIAGRAM

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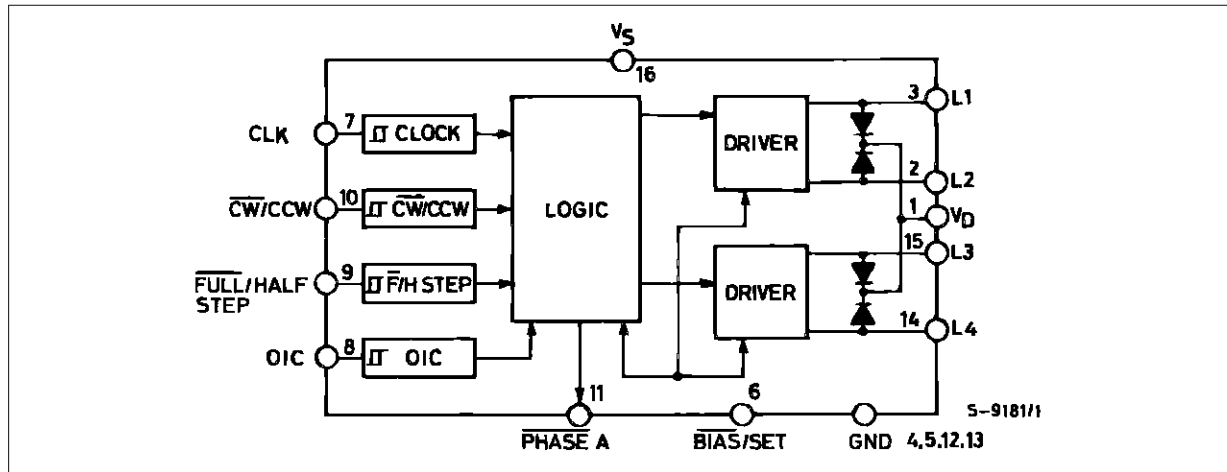
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	16	V_{DC}
V_D	Clamp Diode Cathode Voltage (pin 1)	V_S	V_{DC}
V_{OD}	Driver Output Voltage (pins 2, 3, 14, 15)	V_S	V_{DC}
I_{OD-}	Driver Output Current/Coil	± 500	mA
V_{IN}	Input Voltage (pins 7, 8, 9, 10)	− 0.5 to 7	V_{DC}
I_{BS}	Bias/Set Current (pin 6)	10	mA
V_{OA}	Phase A Output Voltage (pin 11)	16	V_{DC}
I_{OA}	Phase A Sink Current (pin 11)	20	mA
T_j	Junction Temperature	150	°C
T_{stg}	Storage Temperature range	− 55 to 150	°C

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_S	Supply Voltage (DC)	7.2	16	V
V_D	Clamp Diode Cathode Voltage (DC)	–	V_S	V
I_{OD}	Driver Output Current (per coil)	–	350	mA
V_I	DC Input Voltage (pin 7, 8, 9, 10)	0	5.5	V
I_{BS}	Bias/Set Current (outputs active)	− 300	75	µA
I_{OA}	Phase A Sink Current	0	8	mA
T_{amb}	Operating Ambient Temperature	0	70	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	Max.	70	°C/W

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
INPUT LOGIC LEVEL						
V_{TLH}	Threshold Voltage (low to high)				2	V
V_{THL}	Threshold Voltage (high to low)		0.8			V
V_{HYS}	Hysteresis		0.4			V
I_{IL} I_{IH1} I_{IH2}	Current	V_I = 0.4 V V_I = 5.5 V V_I = 2.7 V	− 100		100 20	µA µa µA
DRIVER OUTPUT LEVELS						
V_{OHD}	Output High Voltage	I_{BS} = - 300 µA I_{OD} = - 350mA I_{OD} = - 0.1mA	V_S - 2.0 V_S - 1.2			V
V_{OLD}	Output Low Voltage	I_{BS} = - 300µA, I_{OD} = - 350mA			0.8	V
D_{VOD}	Difference Mode Out Voltage Difference	I_{BS} = - 300µA, I_{OD} = - 350mA			0.15	V
C_{VOD}	Common Mode Out Voltage Difference	I_{BS} = - 300 µA, I_{OD} = - 0.1mA			0.15	V
I_{OZ1}	Out Leakage-HiZ State	$0 < V_D < V_M$, I_{BS} = 5µA	- 100		+ 100	µA
I_{OZ2}	Out Leakage-HiZ State	$0 < V_{OD} < V_M$, I_{BS} = - 300µA Pin 9 = 2V, Pin 8 = 0.8V	- 100		+ 100	µA

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
CLAMP DIODES						
V_{DF}	Forward Voltage	$I_D = 350$ mA		2.5	3	V
I_{DR}	Leakage Current	$V_R = 21$ V			100	μA
PHASE A OUTPUT						
V_{OLA}	Out Low Voltage	$I_{OA} = 8$ mA			0.4	V
	Off State Leakage Current	$V_{OA} = 16.5$ V			100	μA
POWER SUPPLY						
I_{SSB}	Power Supply Current in Stand by State	$V_{BS} = V_S$			12	mA
I_S	Power Supply Current ($I_{OD} = 0$, $I_{BS} = -300\mu A$)	L1 = V_{OHD}, L2 = V_{OLD} L3 = V_{OHD}, L4 = V_{OHD}			75	mA
BIAS SET CURRENT						
I_{BS}	Bias Set Current	to set $\overline{PHASE\ A}$	-5			μA

Notes :   3. DVOD = $\mid$ VOD1.2 - VOD3.4 $\mid$
            VOD1.2 = (VOHD1 - VOHD2) or (VOHD2 - VOLD1) AND   VOD3.4 = (VOHD3 - VOHD4) OR (VOHD4 - VOHD3)
          4. CVOD = $\mid$ VOHD1 - VOHD2 or VOHD3 - VOHD4 $\mid$

AC SWITCHING CHARACTERISTICS ($T_{amb} = 25^oC$, $V_M = 12$ V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CK}	Clock Frequency		0		30	kHz
PWCKH	Clock Pulse Width	HIGH	10			μs
PWCKL	Clock Pulse Width	LOW	20			μs
t_{SU}	Set-up Time $\overline{CW}$/CCW and $\overline{F}$/HS		5			μs
t_{HO}	Hold Time $\overline{CW}$/CCW and $\overline{F}$/HS		10			μs
t_{PCD}	Propagation Delay CLK-to Driver Out			8		μs
t_{PBSD}	Propagation Delay $\overline{Bias}$/Set to Driver Output			1		μs
t_{PHLA}	Propagation Delay CLK-to Phase A LOW			12		μs
t_{PLHA}	Propagation Delay CLK-to Phase A HIGH			5		μs

Figure 1 : AC Test Circuit

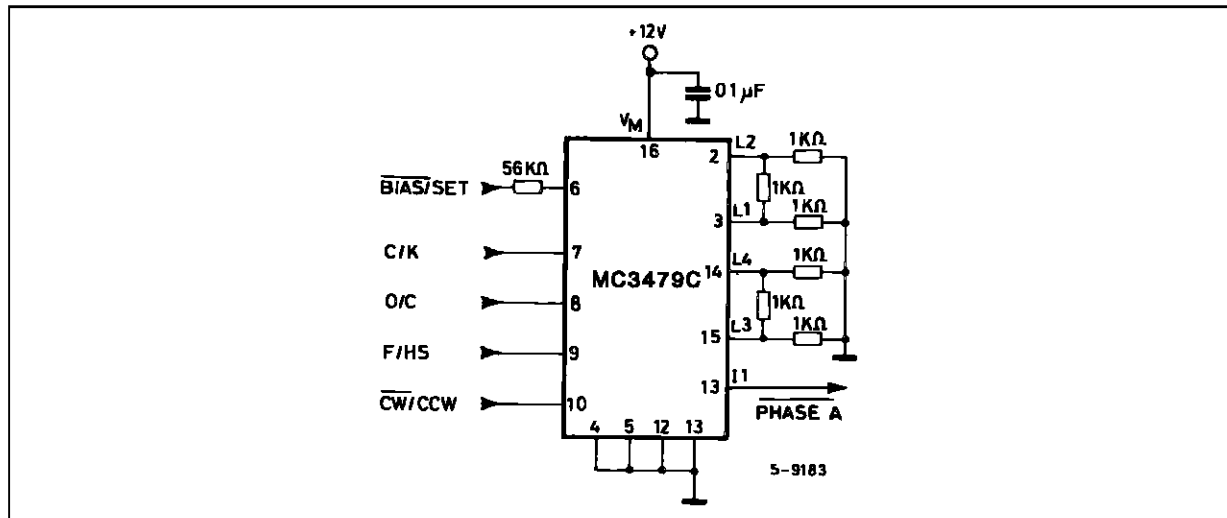**SGS-THOMSON**
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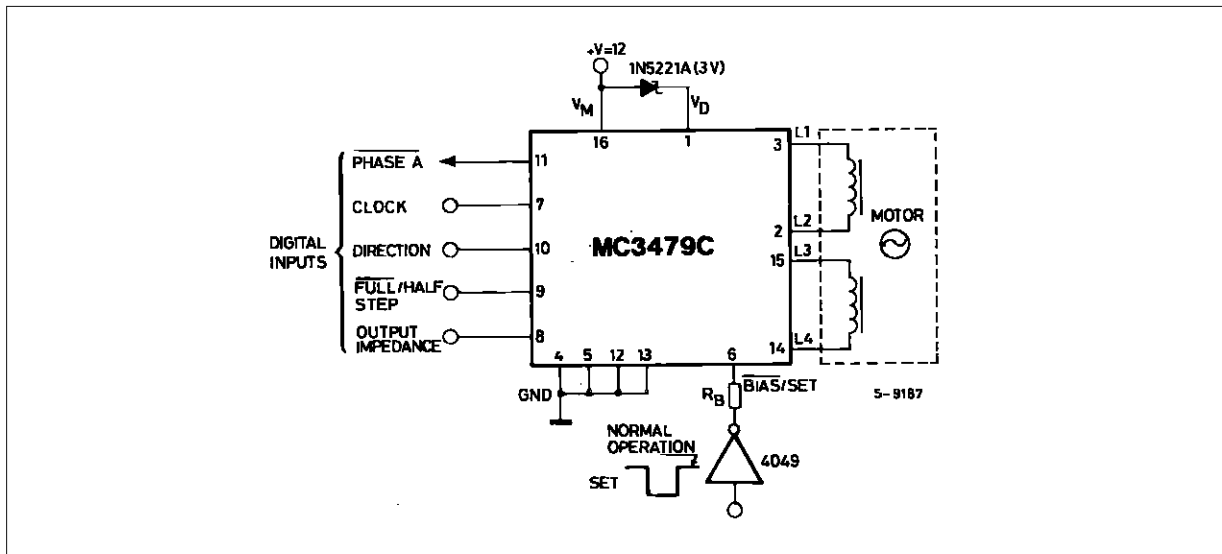
Figure 2 : Typical Application Circuit.

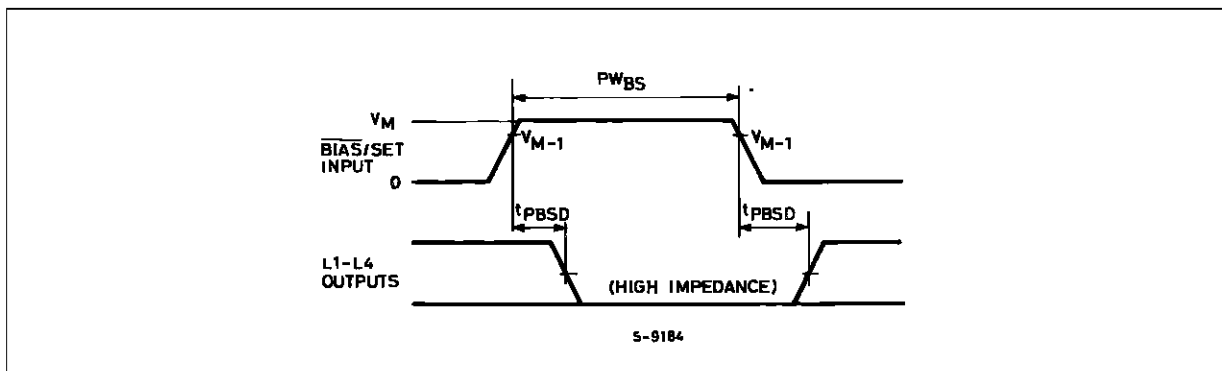**Figure 3** : Bias/Set Timing (refer to fig.1).

Figure 4 : Clock Timing (refer to fig.1).

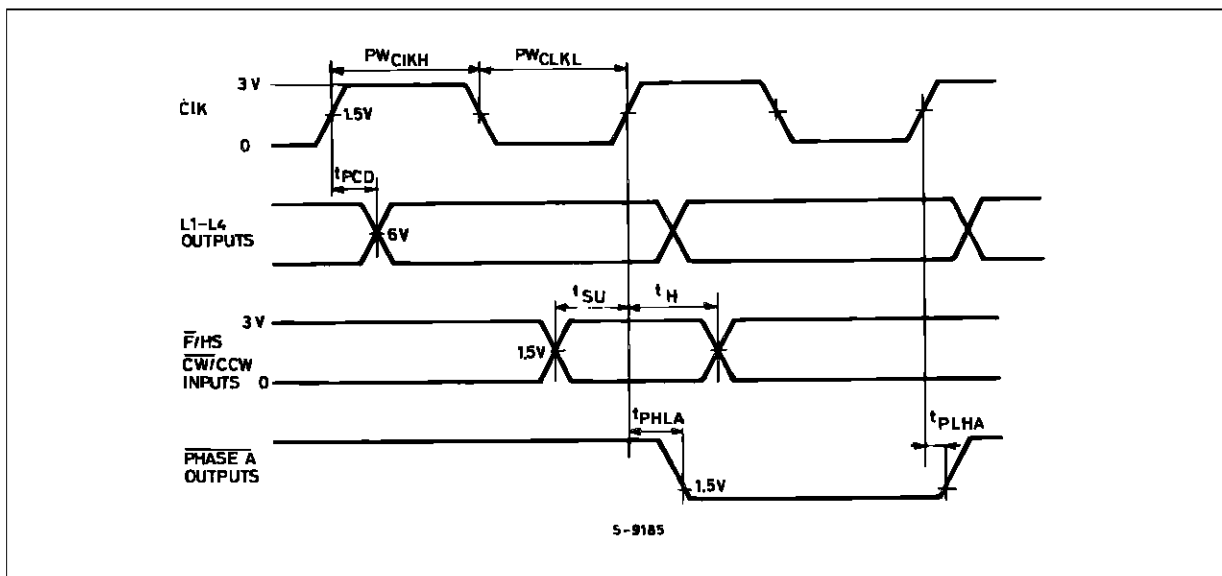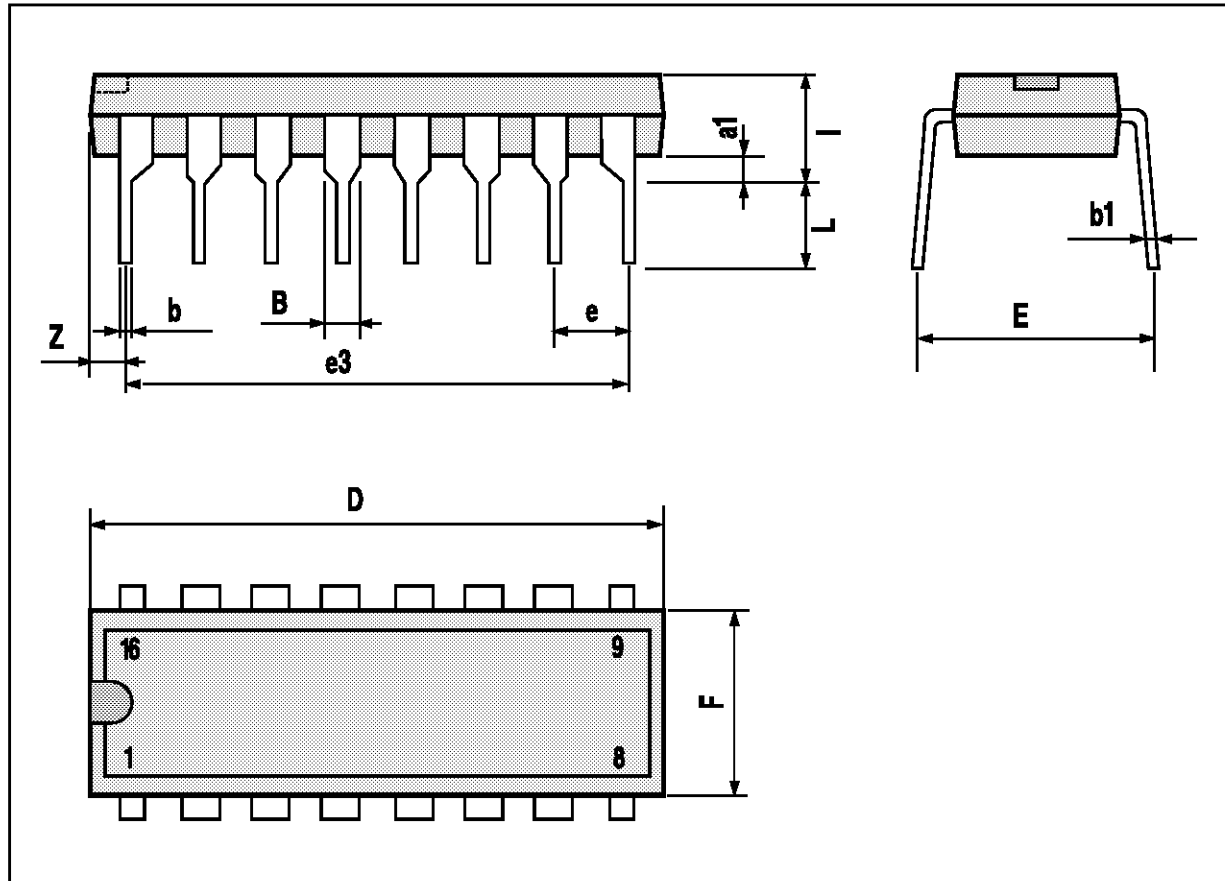**Figure 5 :** Output Sequence.

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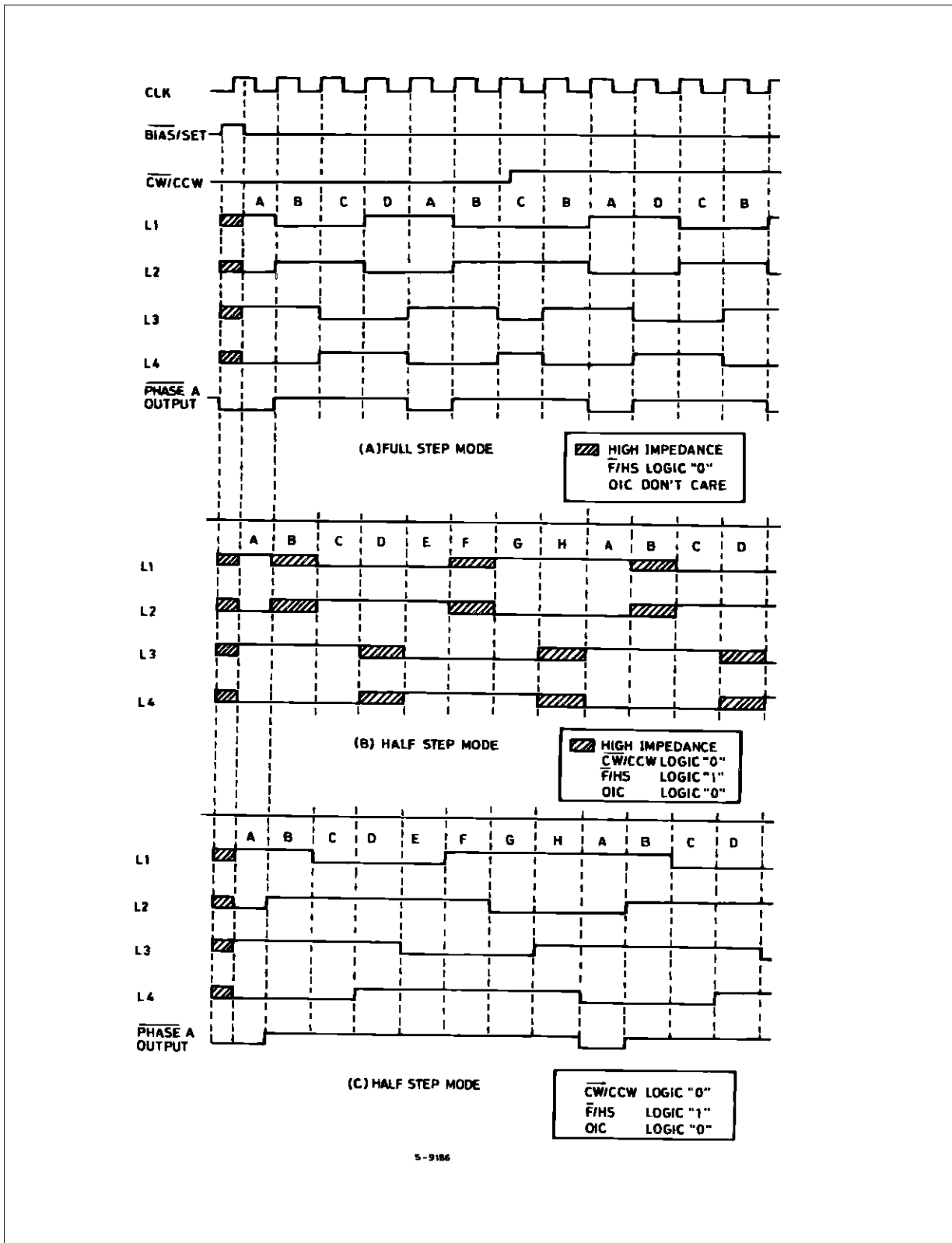
POWERDIP16 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

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